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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,197	KOMODA ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

PD

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 25 July 2005 has been entered. Applicants have cancelled claim 4. Claims 1-3, 5, and 6 are therefore currently pending in this application.

Response to Arguments

2. Applicant's arguments filed 25 July 2005 have been fully considered but do not render the claimed invention non-obvious over the prior art for the reasons set forth below.

Regarding applicant's response the 103(a) rejections: The main thrust of applicants arguments center around arguing that the prior art does not teach modeling Ids-Vds characteristics or a delay library by specifying polygonal lines. The examiner has asserted that applicants claimed polygonal lines are merely disclosed to be "samples" of the Ids-Vds characteristics (i.e. E(t) represented as E1 for a period Δt_1) which are stored in a library. (See: specification page 12, line 12-25) The examiner has interpreted this waveform sampling to be equivalent to the well-known digital sampling techniques (i.e. basic variable rate (VRS) or Nyquist digital sampling of a waveform) where the rate is defined by the period t_n as would have been known to any skilled

artisan. Hence, a skilled artisan would have knowingly incorporated using the same reasoning cited below under 103(a) rejections. Applicant's response has not addressed how the claimed subject matter differs over this interpretation of the claim language. MPEP 2106 recites the following supporting rational for the examiner's interpretation:

> "While it is appropriate to use the specification to determine what applicant intends a term to mean, a positive limitation from the specification cannot be read into a claim that does not impose that limitation. A broad interpretation of a claim by Office personnel will reduce the possibility that the claim, when issued, will be interpreted more broadly than is justified or intended. An applicant can always amend a claim during prosecution to better reflect the intended scope of the claim."

Applicants have also argued that the claimed subject matter can be distinguished over the prior art because by implementation of the claimed delay time estimation method, interpolation errors are reduced, and the size of the library is reduced. However, the claims do not specifically recite any limitations relating to interpretation errors, size of the library, or the reduction thereof. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case applicant's arguments are more specific than the claims require.

The examiner therefore maintains the 35 USC 103(a) rejection of claims 1-3 and 5-6.

The examiner has also now applied new 35 USC 101 rejections to the amended claims. (please see new 101 rejection below) However, applicants are encouraged to contact the examiner and set up an interview for the purpose of resolving such issues.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Specifically, independent claim 1 merely recites the steps of constructing, modeling resistive elements, and segmenting operating characteristics but does not appear to provide (or claim) a delay time estimation result. The Examiner therefore submits that Applicant's have not recited any limitations that provide a tangible result and have merely claimed the abstract process of segmentation operating characteristics of an MOS transistor into regions. No further limitations are recited that provide the actual delay time estimation from the constructing, modeling resistive element, and segmenting steps. Dependent claims 2, 3, 5, and 6 inherit the defects of claim 1.

*An invention which is eligible for patenting under 35 U.S.C. § 101 is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The fundamental test for patent eligibility is thus to determine whether the claimed invention produces a "**useful, concrete and tangible result.**" The test for practical application as applied by the examiner involves the determination of the following factors:*

(1) "Useful" - The Supreme Court in Diamond v. Diehr requires that the examiner look at the claimed invention as a whole and compare any asserted utility with the claimed invention to determine whether the asserted utility is accomplished.

(2) "Tangible" - Applying In re Warmerdam, 33 F.3d 1354, 31 USPQ2d 1754 (Fed. Cir. 1994), the examiner will determine whether there is simply a mathematical construct claimed, such as a disembodied data structure and method of making it. If so, the claim involves no more than a manipulation of an abstract idea and therefore, is nonstatutory under 35 U.S.C. § 101. In Warmerdam the abstract idea of a data structure became capable of producing a useful result when it was fixed in a tangible medium which enabled its functionality to be realized.

(3) "Concrete" - Another consideration is whether the invention produces a "concrete" result. Usually, this question arises when a result cannot be assured. An appropriate rejection under 35 U.S.C. § 101 should be accompanied by a lack of enablement rejection, because the invention cannot operate as intended without undue experimentation.

The Examiner respectfully submits, under current PTO practice, that the claimed invention does not recite either a useful, concrete, or tangible result and is merely drawn to a manipulation of abstract ideas by segmentation operating characteristics of an MOS transistor into regions.

- *The invention is not **useful** since independent claim 1 does not recite a result from the steps of constructing, modeling resistive elements, and segmenting. This makes it difficult to determine Applicant's invention since it merely claims a manipulation of abstract ideas by segmentation operating characteristics of an MOS transistor into regions. (The patent eligibility standard requires **significant functionality to be present to satisfy the useful result aspect** of the practical application requirement. See Arrhythmia, 958 F.2d at 1057, 22 USPQ2d at 1036.)*

- *The claims are not **tangible** since, for example, the results of constructing, modeling resistive elements, and segmenting are undefined. No tangible result is recited as a result of the method steps recited in claim 1.*
- *The claims are not **concrete** because the results are not assured. For example, is a solution possible for any and all arbitrary inputs? (i.e. any segmentation of MOS regions?)*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over "CMOS Gate Delay Models for General RLC Loading", R. Arunachalam et al, Proceedings International Conference on Computer Design, ICCD 97', IEEE 1997, in view of "A Comprehensive Submicrometer MOST Delay

Model and its Application to CMOS Buffers", P. Cocchini et al, IEEE Journal of Solid-State Circuits, Vol. 32, No. 8, August 1997.

Independent claim 1 is drawn to the following elements.

Delay time estimation for logic circuit by:
Modeling MOS transistor by resistive element having
Fixed resistance
Time varying power source voltage
Segmenting modeled MOS transistor characteristic into regions
First region where current increases as gate potential varies
Second (saturation) region where current decreases for constant gate potential
Third (linearity) region where current decreases for constant gate potential

Regarding independent claim 1: Arunachalam discloses a model for delay time estimation of a logic circuit in terms of a time varying voltage source in series with a constant (fixed) resistance (Abstract, page 224, column 2, lines 6&7). Arunachalam teaches the elements of the claimed limitations of the present invention (claim 1) as follows:

Delay time estimation for logic circuit: Arunachalam discloses a model for delay time estimation of a logic circuit. (Pages 226-229, Section 3.3)

Modeling MOS transistor by resistive element: Arunachalam teaches a model for a logic circuit (gate level) that includes a resistive element (fixed resistance). (Abstract, Sections 2&3, pages 226-229, Section 3.3, Figs. 1-5), (See below: Cocchini teaches a transistor level model)

Fixed resistance: Arunachalam teaches a model for delay time estimation in a logic circuit that includes a fixed (constant) resistance. (Abstract, page 225, column 1,

lines 10&11, page 225, Section 3.0, page 226, Section 3.1, page 224, column 2, lines 6&7, Section 4, Figs. 4-10)

Time varying power source voltage: Arunachalam teaches a model for delay time estimation in a logic circuit that includes a time varying voltage source model. (Abstract, page 225, column 1, lines 10&11, page 226, Section 3.2, page 224, column 2, lines 6&7, Section 4, Figs. 4-10)

Arunachalam does not explicitly teach segmenting a transistor model into regions of device operation.

Cocchini discloses a transistor level model for delay time estimation of a logic circuit that includes segmenting the transistor model into regions of device operation including off, saturation, and linearity regions. Cocchini teaches the elements of the claimed limitations of the present invention (claim 1) as follows:

Segmenting modeled MOS transistor characteristic into regions: Cocchini discloses segmenting the transistor model into regions of device operation. (Figure 2, pages 1255-1257, Section III: MOST Delay Model) Cocchini actually teaches beyond the requirements of the claimed limitations of the present invention in that there are five regions but includes the claimed elements of the first, second and third region as a subset. (See below)

First region where current increases as gate potential varies: Cocchini discloses a region where current is increasing as the gate potential varies. For example, in Region 0 of Cocchini, the current is increasing (charging) as the input voltage (and

hence the output voltage (Vo)) increases (i.e. varies). (See: page 1255, column 1, paragraph 4, Section III MOST Delay Model, Equation 7)

Second (saturation) region where current decreases for constant gate potential: Regions 1 and 2 of Cocchini disclose saturation regions of the transistor model. In Region 2, for example, Cocchini discloses a saturation region where the charge is now decreasing (negligible) and Vi is now equal to Vdd (i.e. constant). (See: page 1256, column 1, last paragraph (Section C. Region 2))

Third (linearity) region where current decreases for constant gate potential: Regions 3 and 4 of Cocchini disclose linearity regions of the transistor model. In Region 4, for example, Cocchini discloses a linearity region where the charge is now decreasing (negligible) and input voltage is constant and equal to Vdd. (See: page 1257, column 1, 2nd paragraph (Section E. Region 4))

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Arunachalam relating to a modeling delay time of a logic circuit in terms of a time varying voltage source in series with a constant (fixed) resistance, with the teachings of Cocchini relating to a transistor level model for delay time estimation of a logic circuit that includes segmenting the transistor model into regions of device operation, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many types of delay time estimation techniques available in the market place (see Dagenais Abstract, for example) and large amounts of money being spent in product development and improvement to solve problems arising from modeling logic circuit delays for

increased signal speeds. (See: Cocchini and Arunachalam, Introductions) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Arunachalam with the teachings of Cocchini in order to reduce development time and cost.

Dependent claim 2 is further drawn to:
A circuit of a plurality of logic circuits including MOS transistors by;
Segmenting logic circuit last-stage MOS transistor characteristic into
First region where current increases as gate potential varies
Second (saturation) region where current decreases for constant gate potential
Third (linearity) region where current decreases for constant gate potential

Regarding dependent claim 2: Dependent claim 2 merely requires that the elements of claim 1 relating to segmenting the logic circuit into regions be applied to a plurality of logic circuits comprised of MOS transistors to a final stage logic element. Arunachalam teaches delay time estimation modeling of gate and cell level (multiple logic circuits) logic circuits (i.e. a plurality or logic circuits (all stages)) as noted above. Cocchini discloses a transistor level model (MOS transistors) for delay time estimation of a logic circuit that includes segmenting the transistor model into regions of device operation (saturation, linearity, etc.) as noted above. Accordingly, these limitations are rendered obvious in view of the reasoning and prior art as previously cited above.

Dependent claim 3 is further drawn to:
(E) Powers source voltage = Rs (resistance model of power source) x (i) charge current of load model (t) + (v) charge voltage of load model (t).

Regarding dependent claim 3: The equation of claim 3 requires that the voltage (E) of the power source be equal to the resistance model (Rs) times the charge current

(i) plus the charge voltage (v) of the load model for time ($\Delta t_{1,2}$) required to reach the power source voltage (boundary). (i.e. a time based representation of the fixed resistive element and power source voltage) Arunachalam teaches the resulting gate effects of a time-varying voltage source and a fixed resistive element for a wide range of effective capacitive load values represented as time duration slope ramps (curves) of gate voltage. (See Arunachalam pages 226-229, Section 3.1-4.0, Figs. 4-10, page 227, especially paragraphs 2-6) The examiner further notes that both the source and load models have been disclosed by applicants to be known prior art. (See: specification page 3, lines 6-27)

Dependent claim 5 is further drawn to:
Computer code program medium of claim 1 limitations

Regarding dependent claim 5: Dependent claim 5 merely claims the computer program medium for the program code to perform the method claimed in independent claim 1 and is therefor rejected using the same reasoning as cited above.

Regarding dependent claim 6: Dependent claim 5 merely requires that the delay calculation determine the input slew rate at the last stage of internal delay based in the input rate and an extracted delay parameter. This limitation is rendered obvious in view of Cocchini which teaches that the delay calculation is determined over the entire model, i.e. over all (including final) cells (See: page 1260, Section C).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,066,177 issued to Iwanishi teaches time delay estimation in logic circuits and a delay library.

U.S. Patent 6,606,587 issued to Nassif et al teaches time delay estimation in logic circuits.

U.S. Patent 6,099,576 issued to Jiang teaches time delay estimation in logic circuits.

"Efficent Gate Delay Modeling for Large Interconnect Loads", A.B. Kahng et al, IEEE 0-8186-7286-2/96, IEEE 1996 teaches time delay estimation in logic circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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